Low Dark Current Logarithmic Pixels

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Abstract—The sensitivity of logarithmic pixels at low light levels is limited by the dark current that flows through the load transistor in the pixel in parallel with the photocurrent. A new layout for a logarithmic pixel is reported that significantly reduces the dark current in the pixel. In addition a simple change to the bias voltages applied to the pixel means that the new layout can simultaneously exhibit a linear response to low-light levels and a logarithmic response at higher light levels.

I. INTRODUCTION

Logarithmic pixels are capable of imaging more than 6 decades of illumination. Their dynamic range is therefore significantly higher than that of both CCDs and CMOS based active pixel sensors whose outputs are limited to a dynamic range of less than 3 decades [1]. Another advantage of logarithmic pixels based upon a load transistor operating in subthreshold is that this high dynamic range is represented in a small output voltage range and hence these pixels will be ideally suited to the reduced voltage range of future deep sub-micron processes.

![Fig. 1. A typical logarithmic Pixel](image)

A typical logarithmic pixel is shown in figure 1. In this circuit transistors $M_2$ and $M_3$ act as a source follower-select switch combination to selectively connect the pixel to a shared output line. The logarithmic response of the pixel then occurs because $M_1$ is a nMOS load transistor operating in subthreshold. This means that the output voltage of the pixel is proportional to the logarithm of the current flowing into the source of this device. Ideally, the current flowing through the source of transistor $M_1$ is the photocurrent generated in the photodiode. However, our previous results have shown that there is an additional contribution to the current flowing through the load transistor. This additional contribution, which arises from leakage currents in the photodiode, means that the pixel response saturates at low illuminations and is therefore known as the dark current. The model for the response of this pixel to a photocurrent $x$ in the presence of a dark current $c$ is [1]

$$y = a + b \log(x + c)$$

where $a$ represents the offset voltage of the pixel and $b$ its gain. From this model it is immediately apparent that, as shown in Figure 2, the pixel will only respond to changes in photocurrent when $x > c$. Less obviously, the dark current has an adverse effect on the procedure that is required to compensate for the variations between the offset and gain parameters of individual pixels that give rise to fixed pattern noise. In particular, it has been observed in previous work that fixed pattern noise correction, shown in Figure 3, is only effective for photocurrents that are more than two orders of magnitude larger than the dark current [2]. The dark current therefore has a severe effect on limiting the lowest illumination condition in which a logarithmic pixel can operate successfully.

![Fig. 2. The response of a logarithmic pixel showing the expected loss of any sensitivity to changes in photocurrent at low photocurrents.](image)
modifications are one way to reduce dark currents. However any process modifications can only be undertaken by the manufacturer and are expensive to implement. In this paper a circuit layout is described in section II that uses a polysilicon ring around the photodiode, to reduce the dark current. Experimental results for pixels manufactured in a typical 0.35\(\mu\)m CMOS technology are then presented in section III that show a significant improvement in the maximum dark current within an array of pixels. In the same section it is also shown that by modifying the bias voltages applied to this circuit it is possible to create a pixel that gives a linear response at low light levels and logarithmic response to bright lights.

II. LOW DARK CURRENT STRUCTURES

One of the principal components of dark current is edge leakage currents. These currents owe their origin to defects at the \(n^+\)-diffusion field oxide interface caused by either mechanical stress effects and contamination. Kopley, Vook and Dungan have proposed a biased guard layer, preferably of a conductive material, to block the doping of the active area diode during fabrication in an active pixel sensor[3]. If the guard layer is biased below the threshold voltage for formation of a channel this structure reduces leakage currents by separating the photodiode from the field oxide. Cheng and King have used a similar structure, but have utilised a \(n^+\) reset ring type of structure to reduce the dark current in active pixel sensor[4].

Figure 4 shows the layout of a 10\(\mu\)×10\(\mu\) pixel with a guard ring designed to be manufactured on an 0.35\(\mu\)m process with a fill factor of 40%. In this layout the photodiode has been encircled by the thinnest possible guard ring of polysilicon, to separate the diffusion and field oxide region. This guard ring needs to be biased at a voltage below the threshold voltage of the technology. In an active pixel sensor this guard ring can be used as the reset gate of the pixel to reduce its impact on the fill factor. However, in a logarithmic pixel this reset transistor is replaced by the load transistor that operates in subthreshold. In the logarithmic pixel in a guard ring the photodiode is connected to the load device using a metal bridge across the guard ring which is provided with a separate bias connection. In addition our previous experience of electronic calibration of pixels in this technology has shown that the device leakage currents through nMOS devices with a zero gate-source bias are comparable to the dark current of the photodiodes used. This leakage current however reduces to insignificant values when a negative gate-source voltage in excess of -250\(mV\) is used. In this layout the guard ring around the photodiode therefore acts as the gate of an nMOS transistor in which the acts as the drain and the surrounding region acts as the source. Applying a positive voltage to the bias for the source and a zero voltage to the guard ring will ensure a negative gate-source bias on this guard transistor. Comparison of figure 4 and figure 5 shows that by placing the connection for the source bias of the guard nMOS over the non-photosensitive region of the adjacent pixel it is possible to accommodate the guard structure with a minimum reduction in fill factor. To allow a comparison of the effectiveness of the guard structure a small array of 100×10 pixels of both the kinds have been fabricated on a typical 0.35\(\mu\)m CMOS process from Austria Microsystems.

III. EXPERIMENTAL RESULTS

The strategy that has been used to determine the effective dark current in each pixel in the array is based upon the
technique that has been used previously to determine the offset and gain variations between logarithmic pixels[2]. This technique is based upon the three parameter model of the pixel response.

\[ y = a + b \log(c + x) \]

The offset and gain parameters of each pixel can be calculated using the pixel responses, \( y_1 \) and \( y_2 \), at two photocurrents, \( x_1 \) and \( x_2 \), significantly higher than the dark current. In particular, this means that the lower of these two photocurrents should be approximately one hundred times larger than the maximum expected dark current. This reduces the effect of the dark current on the pixel response to less than 1%. The second photocurrent then has to be significantly larger than the first photocurrent to reduce the effects of temporal and quantisation noise on the calculation of the gain parameter. However, if this second current is too large then the load transistor will be forced to operate in moderate inversion and the simple three parameter model will no longer be valid, hence the high residual fixed pattern noise at large photocurrents in figure 2. Experience has shown that the best strategy is to use a photocurrent that is approximately 300 times larger than the first photocurrent. The offset and gain parameters can then be extracted using the equations

\[ b = \frac{y_1 - y_2}{\log(x_1 / x_2)} \quad (1) \]

\[ a = y_1 - b \log(x_1) \quad (2) \]

The final step in determining the dark current related parameter is then to use these two parameter values and the response of the pixel in the dark, \( y_d \), using the equation

\[ c = \exp\left(\frac{y_d - a}{b}\right) \quad (3) \]

The two photocurrents can be generated by illuminating the array of the pixels with two uniform different light intensities. However, it is more convenient to generate a bias current for each pixel electronically using a calibration current source present in every column[2]. The three parameters of the two arrays of pixels obtained using electronically generated calibration currents are summarised in the table III. As expected the offset and gain parameters of the two different pixels are very similar. It can also be seen that the mean value of dark current related parameter of the layout without the guard ring is approximately half of that of the pixel without guard ring. In addition, the spread of the dark current related parameter has also been reduced to one third of its original value. This means that the worst case dark current in the pixel array is expected to be reduced by a factor of between two and three by using the guard ring. In fact our results showed that in addition to reducing the mean and the standard deviation of the dark current related parameter the presence of the guard ring also eliminated some particularly high dark currents that occurred near the edge of the array of pixels without a guard ring. Using the guard ring therefore reduced the worst case dark current from 2.8fA to less then 0.6fA. The dark current this therefore reduced by a factor of almost five.

<table>
<thead>
<tr>
<th>Parameters of the pixel</th>
<th>without guard ring</th>
<th>with guard ring</th>
</tr>
</thead>
<tbody>
<tr>
<td>Offset (in m V)</td>
<td>668</td>
<td>668</td>
</tr>
<tr>
<td>Gain (in m V/decade)</td>
<td>55.8</td>
<td>56.2</td>
</tr>
<tr>
<td>Bias (in fA)</td>
<td>0.75</td>
<td>0.31</td>
</tr>
</tbody>
</table>

TABLE I

*TABLE OF PARAMETERS*

In addition to reducing the dark current the new pixel layout has a second possible advantage. To reduce the dark current the guard ring is kept at zero bias and the pixel is operated continuously. However, it is also possible to apply a reset pulse on the guard ring. To understand the effect of this consider the equivalent circuit shown in figure 6. This shows that if the gate voltage of the reset transistor is held low the pixel will have a logarithmic response. However, if a positive pulse is applied to the gate the internal capacitance can be reset to a voltage above the gate bias for the load transistor. This will turn off the load transistor. The photocurrent will then discharge the pixel capacitance to create a linear response. However, eventually the voltage in the pixel will fall below the gate bias voltage for the load transistor which will then supply current and an equilibrium will be achieved when the pixel output voltage is proportional to the logarithm of the photocurrent. If the pixel output voltage is measured at a predetermined time after the reset pulse has gone low the pixel will have a linear response at low light-levels and logarithmic response for high light-levels. This response is similar to that reported by Fox, Hynecek and Dykaar[5].

Fig. 6. Equivalent schematics of the layout with guard ring used as a pixel with combined linear and logarithmic response.

To show this new operating mode a pixel with a guard ring has been tested at various electronically generated currents. The first results, in figure 7, show the temporal response of the pixel at three different photocurrents. As expected at low photocurrents, equivalent to low light intensities, the pixel capacitance is simply discharged by the photocurrent until the pixel is reset. In contrast at high photocurrents an equilibrium is quickly achieved and the pixel voltage is constant. The relationship between this constant voltage and the photocurrent is most easily determined by measuring the
pixel output voltage at the end of a constant integration time for different photocurrents. The results in figure 8 clearly show the linear relationship between output voltage and photocurrent at low photocurrents followed by a linear region at higher photocurrents. At the extreme right hand side of the data there is also evidence of the beginnings of a breakdown in the logarithmic response as the load transistor is driven into moderate inversion.

![Graph showing pixel output voltage vs time for different photocurrents.](image)

**Fig. 7.** Response of the pixel as a function of time for three different photocurrents.

![Graph showing pixel response vs logarithmic and linear regions.](image)

**Fig. 8.** Response of the pixel at various photocurrents with fixed integration time

### IV. Conclusion

A low dark current layout for logarithmic pixels has been designed and tested which does not involve any process modification. This structure reduces the dark current in the pixel by a factor between four and five resulting in an improvement in the performance of the logarithmic pixel at low light levels. In addition, simply changing the bias scheme for the guard ring of the new layout converts the pixel to one that simultaneously has a linear response at low light levels and logarithmic response at high light levels.

### References