A Logarithmic CMOS Image Sensor with Adjustable Photo-response

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ABSTRACT
Using logarithm is always a good strategy for representing a high dynamic range signal. However, despite the potentially huge market for any high dynamic range camera, the conventional logarithmic approach using a MOSFET operating in subthreshold mode suffers from low sensitivity especially at low light levels. In this work, a novel high dynamic range pixel with logarithmic response is proposed. Through using an in-pixel comparator and designing the proper reference voltage, up to 110dB dynamic range can be achieved from the measurement results. In addition, there are two major advantages over conventional logarithmic pixel: The first advantage is that the output signal from this pixel is more immutable to temporal noise owing to output voltage swing is enlarged from 0.3V to 2V using 0.35µm process. The other advantage is that the dynamic range can be adjusted by using different shaped reference voltage. Thus, different photo responses for certain applications can be chosen by circuit designers or even users instead of limiting by process.

Keywords
CMOS image sensor, high dynamic range camera, logarithmic pixel, low sensitivity, temporal noise

1. Introduction
The market for solid-state image sensors has been experiencing vigorous growth in recent years due to the increasing demands of mobile imaging, digital still cameras, video cameras, internet-based video conferencing, and surveillance systems. With over 350 million parts shipped in 2005 and an estimated annual growth rate of over 30%, image sensors have become a significant market that is driving the development of silicon technology. Charge-coupled device (CCD) image sensors have traditionally been the dominant image sensor technology. With the rapid advances in complementary metal oxide semiconductor (CMOS) technology, the evolution of image sensors based on CMOS process has been the subject of many studies in the past ten years [1-3]. Compared to charge couple devices (CCDs), the advantages of CMOS imagers are lower supply voltage, lower power consumption, and an ability to integrate other CMOS circuitry that enables highly integrated image sensors to be manufactured to lower cost. These advantages have meant that CMOS cameras have become increasingly competitive in recent years. One of the key performance attributes of both CCD and CMOS digital cameras that needs to be improved is their dynamic range.

The dynamic range of conventional CMOS image sensor, 55 to 65dB, is still incapable of capturing natural scenes. There are two directions which could lead to dynamic range improvement. One is to reduce the dark current level and extend the DR towards darker scenes and various approaches have been proposed to minimize the dark current level [4-7]. However, the standard CMOS process is not designed for imaging; hence the improvement is rather slight. The other is to improve the dynamic
range towards brighter scenes by extending the incident light saturating level. The maximum detectable signal of a conventional active pixel sensor is primarily limited by low power supply and linear integration. Many methods to expand the dynamic range of CMOS image sensors have been reported [8]. One popular approach is multiple sampling which expands the dynamic range of image sensor by sampling the response of each pixel several times to avoid saturation [9-11]. Although this is an evolutionary approach that builds upon well understood principles and techniques, the main problem is the large number of bits per pixel needed to represent an image that have to be stored and displayed. Another method of obtaining a wide dynamic range is to use logarithmic compression [12-14]. Logarithmic pixels have been manufactured by several groups that possess a wide dynamic range and it is possible to correct the fixed pattern noise that degrades the quality of the images. However, these logarithmic pixels suffer from a low sensitivity, especially at low light levels, which makes them vulnerable to temporal noise.

In this paper, a novel logarithmic response CMOS active pixel sensor (APS) with improved sensitivity is presented. Instead of using transistors operated in subthreshold region, the logarithmic photoresponse is successfully achieved using linear integration. The dynamic range of the proposed pixel is extended up to 110dB and it has two major advantages over conventional logarithmic pixel with subthreshold load: The first advantage is that the output signal from this pixel is more immune to temporal noise owing to its larger output swing. The other advantage is that the photo response can be adjusted by using different shaped reference voltages.

2. Design of the Pixel

A circuit diagram of the proposed sensor pixel and its operation timing diagram are shown in Figure 1. A logarithmic response is achieved by integrating an in-pixel comparator and a PMOS switch (M2) into each pixel. The comparator and the switch are connected so that when the voltage $V_{\text{diode}}$ is higher than the reference input voltage to the comparator, $V_{\text{ref}}(t)$, the comparator output is low and the switch is turned on. However, when $V_{\text{diode}}$ is less than $V_{\text{ref}}(t)$, the comparator output will be high and the switch will be turned off. The gate of the source follower transistor M3 will then be isolated from the photodiode. That is to say the voltage sensed at the output node, $V_{\text{out}}$, at the end of an integration period will depend on the value of $V_{\text{diode}}$ when $V_{\text{diode}} = V_{\text{ref}}(t)$. As in the conventional linear pixel, the process of forming an image starts when $V_{\text{diode}}$ is reset to a high voltage, in this pixel $V_{\text{dd}} - V_{\text{th,M1}}$ (threshold voltage of M1), by applying a high reset voltage, $V_{\text{dd}}$, to the gate of reset transistor M1. When the reset voltage goes low the transistor M1 stops conducting and the photocurrent starts to discharge the diode capacitor $C_{\text{diode}}$. This means that at a time t seconds after the reset voltage has gone high:

$$V_{\text{diode}} = V_{\text{dd}} - V_{\text{th,M1}} - \frac{I_{\text{ph}} t_s}{C_{\text{diode}}} \quad (1)$$

This voltage is compared by the comparator with the time dependent reference voltage $V_{\text{ref}}(t)$. The output of this comparator
is then connected so that it connects the gate of the source follower transistor M3 and the photodiode when \( V_{\text{diode}} < V_{\text{ref}}(t) \). Ideally, the readout circuit will sample the output voltage as soon as \( V_{\text{diode}} = V_{\text{ref}}(t) \). Consequently, different relationships between the pixel output voltage and the photocurrent can be obtained using different reference voltages for \( V_{\text{ref}}(t) \).

In the context of logarithmic response, the aim will be to stop the integration process at a time \( t_s \) so that the change in output voltage is proportional to the logarithm of the photocurrent \( I_{\text{ph}} \). Assuming the photocurrent is being integrated onto the diode capacitance \( C_{\text{diode}} \). This means:

\[
V_{\text{ref}}(t_s) = V_{\text{diode}}(t_s) = V_{\text{dd}} - V_{\text{th,M1}} - \frac{I_{\text{ph}} t_s}{C_{\text{diode}}}
\] (2)

to get a logarithmic response with slope \( S \):

\[
V_{\text{ref}}(t_s) = V_{\text{dd}} - V_{\text{th,M1}} - S \ln \left( \frac{I_{\text{ph}}}{I_{\text{ref}}} \right)
\] (3)

then the time to stop the integration can be expressed as:

\[
t_s = \left( \frac{S C_{\text{diode}}}{I_{\text{ph}}} \right) \ln \left( \frac{I_{\text{ph}}}{I_{\text{ref}}} \right)
\] (4)

Figure 2. Comparator input simulated in MATLAB model

The MATLAB simulated comparator input signal, \( V_{\text{ref}}(t) \), required to generate a pixel output voltage that is proportional to the logarithm of the photocurrent using typical 0.35 \( \mu \)m process parameters is shown in Figure 2. Figure 3 illustrates the time at which integration stops as a function of the photocurrent. It is found that a lower illumination level, i.e. smaller photocurrent, leads to a late comparator switching and hence a longer integration time. This means the proposed pixel uses an illumination-level adaptive integration time to extend its dynamic range.

3. Experimental Results

A prototype of the proposed pixel with logarithmic response has been designed and simulated using the Cadence Spectre simulation tool. Almost all the transistors in the pixel, including those in the comparator, are 1\( \mu \)m wide and 0.6\( \mu \)m long. The only exception was M3 which is 5\( \mu \)m wide and 1\( \mu \)m long to increase the capacitance that stores the sampled voltage to reduce the effect of leakage and clock feed through from the switch transistor.

Figure 3. The time at which integration stops

In Figure 4, the simulated photo-response of the proposed pixel is compared with that of conventional logarithmic pixel with a subthreshold load, also simulated using the parameters for a 0.35\( \mu \)m 3.3V Austria Microsystems CMOS process. As expected, the response to photocurrents of the proposed pixel is found to be
logarithmic and the total dynamic range of operation is found to be extended more than 50dB in comparison with conventional three-transistor linear pixel. The minimum detectable photocurrent is found to be 200 fA, while the pixel remain logarithmic to photocurrents as high as 80 nA. These results show the one critical advantage of this approach over the conventional method of creating a logarithmic pixel is that the change in output voltage per decade change in photocurrent is more than 250mV/decade, compared to less than 60mV/decade in the conventional logarithmic design. This is significantly more than the sensitivity of the conventional logarithmic pixel based upon a load transistor in weak inversion. The new design will therefore be more robust to temporal noise.

The proposed logarithmic pixel was fabricated using the AMS 0.35µm standard CMOS logic process. The pixel size and fill factor of the prototype are 25 by 25 µm$^2$ and 24%, respectively. In order to simplify experiments and test the pixel photoresponse electronically, a calibration pixel was fabricated. In this pixel a bias controllable current source, M5, was substituted for the photodiode as illustrated in Figure 5. The reference voltage used for the comparator input is provided by an Agilent IntuiLink Waveform Editor and a 33250A arbitrary waveform generator. The corresponding photocurrent values at different tested bias voltages, $V_{\text{cal_in}}$, are estimated from the Cadence Spectre simulation results.

### 3.1 Pixel Circuit

The proposed pixel can function as a conventional linear pixel when the output voltage of the in-pixel comparator is kept low, i.e. the PMOS switch is turned on, throughout the integration period. Therefore, the functionality of the reset transistor as well as the readout circuit can be examined by setting $V_{\text{ref}}(t)$ to a low voltage, 0V.

![Figure 5. Schematic of the calibration pixel with a bias controllable current source](image)

**Figure 6. Measured output voltage of the proposed pixel in linear mode**

The measured output voltage of the pixel in this operation mode is shown in Figure 6. After the reset transistor is turned off, the output voltage starts to fall linearly and the rate of change depends on the magnitude of the applied photocurrent. It is also found that the output voltage saturates to 0V when larger photocurrents are applied. This means the photoresponse of the proposed pixel to different photocurrents is identical to that of conventional linear pixel.

### 3.2 Comparator

The comparator consists of a PMOS input differential stage and bias circuit as illustrated in Figure 7. Due to the low operating voltage and the desire for a large input swing, the folded-cascode architecture is used. In addition, this architecture is adopted with a self-biased current source. The functionality of the comparator was electrically tested by applying different constant voltages as the comparator input and measuring the resulting output as illustrated in Figure 8. The measurement result shows a good linearity as that in simulation result. The output voltage stays at 0V when a $V_{\text{ref}}$ smaller than 0.65V and 0.7V is applied from simulation and measurement results, respectively.
Figure 7. In-pixel comparator circuit diagram

Figure 8. Illustration of the constant $V_{\text{ref}}$ and the measurement result of comparator linearity

This value is determined by the threshold voltage drop in the readout circuit and the predetermined source follower bias, 1.1 V in this case. It is also found that the extracted slope of the response is approximately 0.8 which within the reasonable range of the simulated source follower gain.

3.3 Dynamic Range

To verify the wide dynamic range operation scheme, the 30-point reference voltage generated from the MATLAB was used as the comparator input. The measured photoresponse of the proposed pixel with this voltage is shown in Figure 9. As required, the pixel shows a logarithmic relationship between the output voltage and input current. The overall dynamic range of the response with this reference voltage covers 5 decades from apico-amperes to a few hundred nano-amperes. The only difference between the simulation and measurement results is an offset. This could arise from a combination of differences between the electronically generated photocurrent and the simulated photocurrent value and threshold voltage variations between devices within pixels.

Figure 9. The measured response of a pixel compared to the simulated response of the pixel

Again, the measurement results prove that a major advantage of this approach over the conventional method of creating a logarithmic pixel is that the change in output voltage per decade change in photocurrent, the slope, is more than 250 mV/decade, compared to less than 60 mV/decade in a conventional design. This means the output voltage will be less vulnerable to both temporal noise and variations between pixels. These pixels will therefore be able to provide a higher quality image.

Another advantage of the proposed pixel is that by using different functions for $V_{\text{ref}}(t)$ it is possible to modify the response of the pixel. An extreme example of this is using a constant, low value, for the reference voltage it is possible to obtain a linear response. A more subtle change is to change the value of the S parameter to control the slope of the photoresponse.

Figure 10 illustrates the measurement results of the proposed pixel using three different reference voltages. It is found that the change
in output voltage per decade change in photocurrent is 480mV/decade, 360mV/decade, and 250mV/decade, respectively. This means that different photo responses can be chosen by the designer or user through tuning the reference voltage to optimize the response of the pixel for a particular application. Furthermore, even wider dynamic range can be achieved when different $V_{\text{ref}}(t)$ is applied.

Therefore, the inaccuracy results from the approximation must be taken into account. The 5, 10, 20, and 30 points reference voltages used to estimate the maximum inaccuracies are shown in Figure 11. The inaccuracy is defined by the error between the output voltage response and an ideal logarithmic response expresses as an error percentage equivalent percentage change (see Figure 12). The maximum error percentage of the $V_{\text{ref}}(t)$ approximated by lesser points is expected to be larger owing to the poorer approximation.

3.4 Reference Voltage

The reference voltage $V_{\text{ref}}(t)$ used in circuit simulation was a 30 points evenly voltage-spaced signal generated by MATLAB. This number of points was limited by the voltage source provided within the simulation tool Cadence Spectre. Specifically, a piece-wise linear waveform is used to approximate the function of the reference voltage required for a real logarithmic response.

The measurement results in Figure 13 show that the maximum percentage error is significantly increased from 4% to 30% when the number of approximation points drops from 30 to 5. Consequently, the maximum acceptable inaccuracy must be investigated and defined before the future design of an integrated reference voltage generator.
4. Conclusions

A novel logarithmic response pixel design for wide dynamic range CMOS imaging has been proposed and described. The pixel has been demonstrated, from both the simulation and measurement results, to have a dynamic range of more than 110dB. Compared to conventional logarithmic pixels with subthreshold load, the proposed pixel has two major advantages: Firstly, the output signal from this pixel is more immune to temporal noise because the output voltage swing is enlarged from 0.3V to 1.7V. The second advantage is by using different reference voltages, it is possible to obtain different photoresponse. The major drawback of this pixel is its large pixel size and low fill factor resulting from the in-pixel comparator. Therefore, further work is required to create a smaller pixel with the same response characteristics.

5. References