A 200MHz analogue-ROM based direct digital frequency synthesiser with amplitude modulation

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Abstract
A novel, low power frequency synthesiser system with 60MHz output bandwidth is reported which is suitable for integration in a single chip RF transceiver. The system is based upon a conventional DDFS architecture. However, the problems which usually arise from the non-ideal behaviour of the DAC and the high power consumption of a ROM are avoided by using a non-volatile analogue memory array. Simulation results are presented which show that the system is suitable for use in an RF transceiver.

I. INTRODUCTION
With the explosion in the mobile telecommunications market over the past few years, there is increasing pressure to develop flexible, smaller, low cost and low power transceivers[1]. This objective can be achieved by integrating as much of the transceiver as possible on a single chip. However, this chip must support both the analogue RF functions and the increasing amount of digital processing required by new air-interface standards. In existing systems, the RF functions are implemented in GaAs chips whilst the digital processing is supported on silicon. This would suggest it will be difficult to develop a single chip transceiver. Fortunately, CMOS circuits have already been shown to operate at 1GHz and future shrinkage of device size will mean that operating frequencies up to 5GHz will be possible[2]. With this emerging technology, the remaining challenge is to find an efficient implementation of each transceiver function suitable for integration in a single chip.

One of the key functions of a transceiver which must be supported is frequency synthesis. A direct digital frequency synthesiser (DDFS) together with a digital-to-analogue converter (DAC) forms a suitable interface between the digital and the analogue domains of a transceiver.

In this paper, a novel low power frequency synthesiser architecture which is based upon DDFS is presented. The system requirements for the synthesiser are first presented. A conventional DDFS architecture is then described together with the problems with implementing this architecture at high frequencies. This is followed by a description of the new DDFS architecture. Finally, results for the proposed DDFS architecture simulated with the parameters from a 0.35μm CMOS process are presented.

II. SYSTEM REQUIREMENTS FOR SYNTHESISER
Many transmitter architectures have quadrature channels (I/Q) to support various digital modulation schemes. These tend to suffer from phase and gain mismatches without complex, power hungry feedback systems. A conventional DDFS architecture is only able to minimise phase mismatch in transmitter I/Q channels. However, this may leave an uncorrected gain mismatch of more than 2% which would cause unacceptable interchannel interference[3]. In contrast, the new frequency synthesis system has been designed to allow the amplitudes of the I/Q channel signals to be matched to within 1%

Another potential advantage of the new frequency synthesis system is that it was developed specifically to have a smaller power consumption than previous designs. This will be particularly important for micro and pico cellular mobile communication systems such as PACS(American) and PHS(Japanese) which have relatively small transmission power levels. The initial aim has therefore been to design a system which is compatible with the PACS standard. This requires a frequency syntheser with an output bandwidth of 60MHz and frequency resolution of 100kHz. In addition, to avoid interference any spurious outputs should be less than -55dBc.

III. CONVENTIONAL DIRECT DIGITAL FREQUENCY SYNTHESISER
A conventional DDFS architecture as originally proposed by Tierney, [4], consists of three major components; an adder-accumulator, a read-only-memory (ROM) and a digital-to-analogue converter (DAC) as shown in Figure 1. Every clock cycle, the adder adds an L-bit digital input word, , to the contents of the accumulator. The result, which is the phase of the waveform, is then stored in the accumulator. Every time the accumulator overflows, a new period of accumulation starts with the overflow remainder in the accumulator. W-bits of the accumulator output then form the address used by the ROM to convert the phase into a digital amplitude signal. The resulting S-bit digital signal is converted into an analogue output by the DAC. Finally, the analogue signal is low-pass filtered to remove the high order harmonics caused by the sample and hold effect of the DAC.
The advantages of DDFS are high frequency resolution and continuous phase switching[5]. These allow a DDFS system to support digital phase and frequency modulation which are important in modern modulation schemes. While DDFS provides the above features, its use has been restricted in mobile communications because of unacceptable spurious outputs and high power consumption especially at high frequencies[5].

The problems of implementing this architecture to give the output bandwidth required in mobile transceivers have been highlighted by Samueli and Nicholas[6]. The DDFS system was designed to give a theoretical spurious output of -90dBc before the DAC. However, non-idealities in the DAC resulted in a real performance of -67dBc at low frequencies of around 1MHz. At higher frequencies the output is expected to deteriorate considerably. This clearly demonstrates that the DAC is responsible for spurious outputs which are difficult to predict and would cause unacceptable interference in a PACS system at frequencies higher than 1MHz. Most of the power is consumed in the conversion of phase information into amplitude that utilises a large ROM and additional logic circuits. The total power dissipation was found to be 1W which is unacceptable for use in mobile communications. Other previous designs have also suffered from high power consumption[7], [8].

IV. NOVEL DDFS ARCHITECTURE

Our approach to solve the problems of power consumption in the ROM and DAC non-linearities involves combining these two functions. In order to achieve this we propose a system, shown in Figure 2, based upon floating-gate analogue memory technology which has previously been used for various applications[9], [10].

The new circuit consists of an array floating-gate MOSFET current sources which are selectively connected by a switch to a common load transistor. The input to this circuit is therefore the control signal which selects the floating-gate device which corresponds to the phase represented by the contents of the accumulator.

Equating the saturation currents of the load and selected floating-gate transistor, \( I_{load} \) and \( I_{fg1} \), leads to an expression for the output voltage,

\[
V_{out} = V_{dd} - V_{T,load} + \alpha (V_{T,fg1} - V_{fg1}) \tag{1}
\]

where \( \alpha = \sqrt{3I_{fg1}} \). Equation 1 shows that the output voltage is proportional to the floating-gate voltage \( V_{fg1} \), scaled by the factor \( \alpha \). Thus \( V_{fg1} \) can be programmed to generate an output voltage corresponding to a particular phase. This suggests that an array of floating-gate devices can be used to replace the ROM+DAC. However, Equation 1 is based upon a simple model of the MOSFET. More detailed circuits simulations are therefore required to assess the impact of phenomena not included in this equation such as switching transients and both back-gate and short-channel effects.

V. SIMULATION RESULTS

The ultimate aim is to construct a DDFS system which can be incorporated within a single chip RF transceiver. Simulations were therefore performed using the device parameters from an \( 0.35\mu m \) CMOS technology.

In order to assess the impact of second order effects, a simple three transistor circuit was simulated with a load capacitance of \( 100fF \) representing the subsequent mixer. Within this circuit, one transistor was used to represent the load device, the second transistor represented the closed switch and the third transistor whose gate was driven by a sine wave generator, represented the array of floating-gate devices.

For the \( 0.35\mu m \) process, the maximum supply voltage is 3.3V and the threshold voltage is 0.5V. Therefore, to ensure operation in saturation, the amplitude of the sine-wave generator was set to between 1.5V and 2.5V. In order to be compatible with the next stage of a complete transmitter, a mixer, the circuit was designed to have an output amplitude of \( 50mV(\alpha = 0.1) \).

Initial simulations were performed with a sine-wave generator frequency of \( 1MHz \). With minimum geometry devices used for the switch and input transistors, the load transistor width was set to \( 6.5\mu m \) to give an output amplitude of \( 50mV \), corresponding to \( \alpha = 0.1 \). Once the geometry of the various devices had been determined a second simulation showed that the circuit was capable of generating a
60MHz output with only a negligible, 70µV, change in amplitude. This circuit is therefore capable of generating the frequencies required by a PACS/PHS system.

One disappointing aspect of these simulation results was that they showed that non-linear effects not included in Equation 1 resulted in unacceptable spurious outputs at a number of the harmonics of the driving input. For example, as shown in Figure 3 for the 1MHz input, the worst-case spurious output was -22.4dBc at 2MHz. Fortunately, in a real system each floating-gate device will be programmed to give the output voltage corresponding to a particular phase. Thus programming of these devices will compensate for both any circuit non-linearity and variations between devices.

In order to remove the effects of the non-linearity and investigate possible switching transients, a circuit consisting of an array of floating-gate devices, together with the corresponding switches and the load transistor and capacitor was simulated. Within these simulations, each floating-gate device was represented by a minimum geometry MOSFET together with a capacitor which represented the total capacitance of the floating-gate. The final aim is to create a system which is capable of generating frequencies up to 60MHz. It was therefore decided to design a system with a clock frequency of 200MHz. For practical reasons, the system was then simulated at a number of frequencies which required the repeated sampling of a relatively small number of different phases.

At the beginning of each simulation, the bias condition on each floating-gate was initialised to the value required to achieve the output voltage at the corresponding phase. The output frequency spectrum of a simulation representing the synthesis of a 25MHz signal is shown in Figure 4. As expected, the harmonics due to the non-linear effect in the previous simulation are reduced considerably, for example the second harmonic when generating 25MHz reduced from -21dBc to -43dBc.

Simulation results above have demonstrated the circuit’s function as a ROM+DAC replacement in a DDFS system. However, it is also necessary to amplitude modulate the output in order to minimise the I/Q channel gain mismatch errors. Equation 1 suggests that the single load transistor can be replaced by several different transistors which can be digitally selected to provide a varying amplitude output. Unfortunately, because of the non-linear transfer characteristics of the circuit, simulations showed that changing the load device caused unacceptable levels of spurious output.

Another circuit has therefore been designed which allows amplitude modulation. The circuit, shown in Figure 5, consists of a source follower, being driven by the output of the original circuit, followed by 5 PMOS transistor pairs. The first PMOS pair generates 100% of the current. The other 4 pairs, controlled by digital signals, are scaled so as to generate 1%, 2%, 4% and 8% of the current. The output current is designed to drive an external 50Ω load. The digitally controlled switches and the input transistors are designed to operate in the saturation region so that any voltage variations on the output drain node do not affect the expected output current.

The frequency spectrum together with the 100% of the output is shown in Figure 6. The worst case spurious output is the second harmonic with a magnitude of -53dBc. The 115% output response, Figure 7, shows a worst case spurious output of -55dBc suggesting that the output spectrum does not deteriorate with amplitude modulation. Analysis of both output waveforms showed that the transient re-
response of floating-gate MOSFETs carrying different currents were not identical because of different operating conditions of the current sources. In order to minimise this effect, the width of floating-gate MOSFETs were modulated relative to the current they were generating. The programming voltage had to be changed to compensate. This ensured that all the floating-gate MOSFETs had similar gate voltages and hence similar operating conditions.

After modification, the result is a worst case spurious output level of -59dBc as shown in Figure 8. This result suggests that the modified circuit together with amplitude modulation is suitable for use in a PACS/PHS mobile terminal. Furthermore, the maximum power dissipation of the circuit is only 35mW which is significantly less than previous art[5].

VI. SUMMARY

A DDFS system is ideal for creating the baseband modulated output in an RF transceiver. However, with current technology, the non-ideal behaviour of the DAC creates undesirable outputs. A novel analogue ROM based DDFS architecture capable of amplitude modulation has been proposed. Results presented have shown that using amplitude modulation, the circuit is able to compensate for I/Q channel gain mismatch to within 1% without loss of performance. The circuit has low power dissipation at high frequencies and the spurious output power is less than -55dBC which is acceptable for use in a PHS/PACS mobile transceiver. Future work is expected to reduce this further.

REFERENCES